

LVTTL SLSC Module



Product Data Sheet
B&A Document 110022_B

Part No.200103_A
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LVTTT SLSC MODULE SPECIFICATIONS



INTRODUCTION

This document contains technical specifications for the LVTTT Module (B&A Part No. 200103_A). Specifications are shown at 25 °C temperature, unless otherwise noted. The main features of the module are listed below:

- Separate 32 Transmit and 32 Receive LVTTT full duplex channels
- Configurable grounding
- On-board isolated voltage regulation
- Internal House Keeping / Health Monitoring
- User controlled Flight interface power on/off
- Built-in LabVIEW FPGA Debugging Port
- Safe to connect to Flight hardware, FMEA approved
- LabVIEW drivers



DIGITAL I/O

Front Panel Connectors	2 x VHDCI (Tables 1 & 2)
Channels Per Connector ¹	32
Maximum Nominal Data Rate of TX and RX Channels	32 Mbit/s
Number of LVTTT TX Channels	32
Number of LVTTT RX Channels	32
Backplane Connectors	3 x SLSC (Tables 3-5)
TX LH Propagation Delay (ns) ² Min, Avg, Max	16, 18, 20
TX HL Propagation Delay (ns) ² Min, Avg, Max	16, 18, 20
RX LH Propagation Delay (ns) ² Min, Avg, Max	16, 18, 20
RX HL Propagation Delay (ns) ² Min, Avg, Max	16, 18, 20

Note:

- (1) All 32 channels (TX and RX) are trace matched and have same delay on the board.
- (2) See Page 4 for propagation delay definitions. Values are measured @ 1 Mhz. / 3.3V.



SAFETY

The following items must be considered for safety:

- Using the LVTTT Card in a manner not described within this document may impair the protection the LVTTT Card provides.
- The SLSC-12001 chassis and the SLSC cards **do not support** hot plug-in. The entire chassis must be powered down when a module is installed.
- Always follow ESD procedures for handling.
- If cleaning is required, wipe with dry and clean towel.
- Installation of the LVTTT SLSC card must be performed in accordance with B&A “Digital Isolation Module User Manual” (Document No. 140020).



SPECIFICATIONS

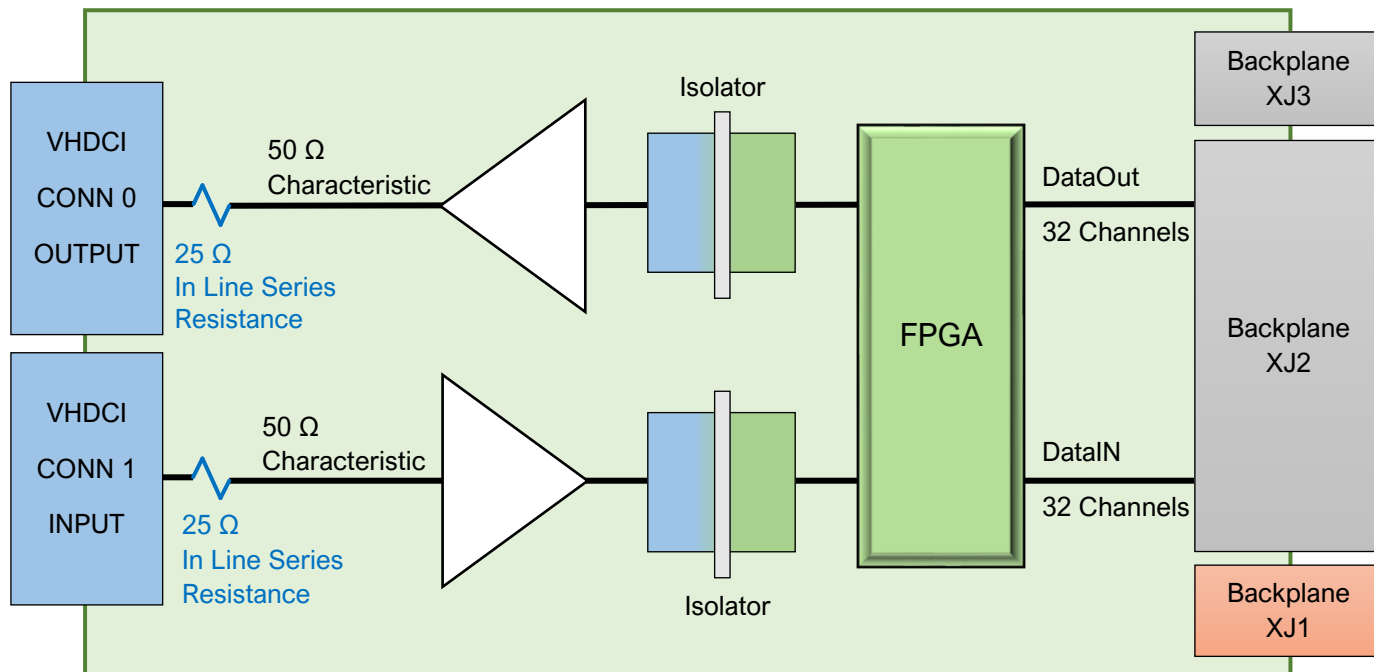
Direction Control of Data Channels	Full Duplex
Power Up State	Drivers and receivers disabled
I/O Compatibility	LVTTT (single ended)
Characteristic Impedance	50 Ω nominal
In Line Series Resistance	25 Ω nominal
Maximum Input Single Ended Voltage	5V
Voltage Level Compatibility	5V input tolerant 3.3V output
Number of Onboard Temperature Sensors	4
LabVIEW FPGA Debug Interface	Micro-USB
Grounding Configuration	See Page 3

DATA SHEET



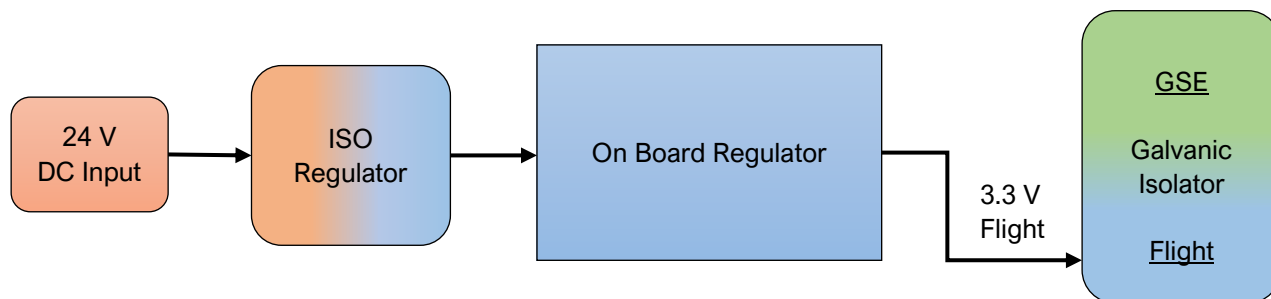
FUNCTIONAL BLOCK DIAGRAM

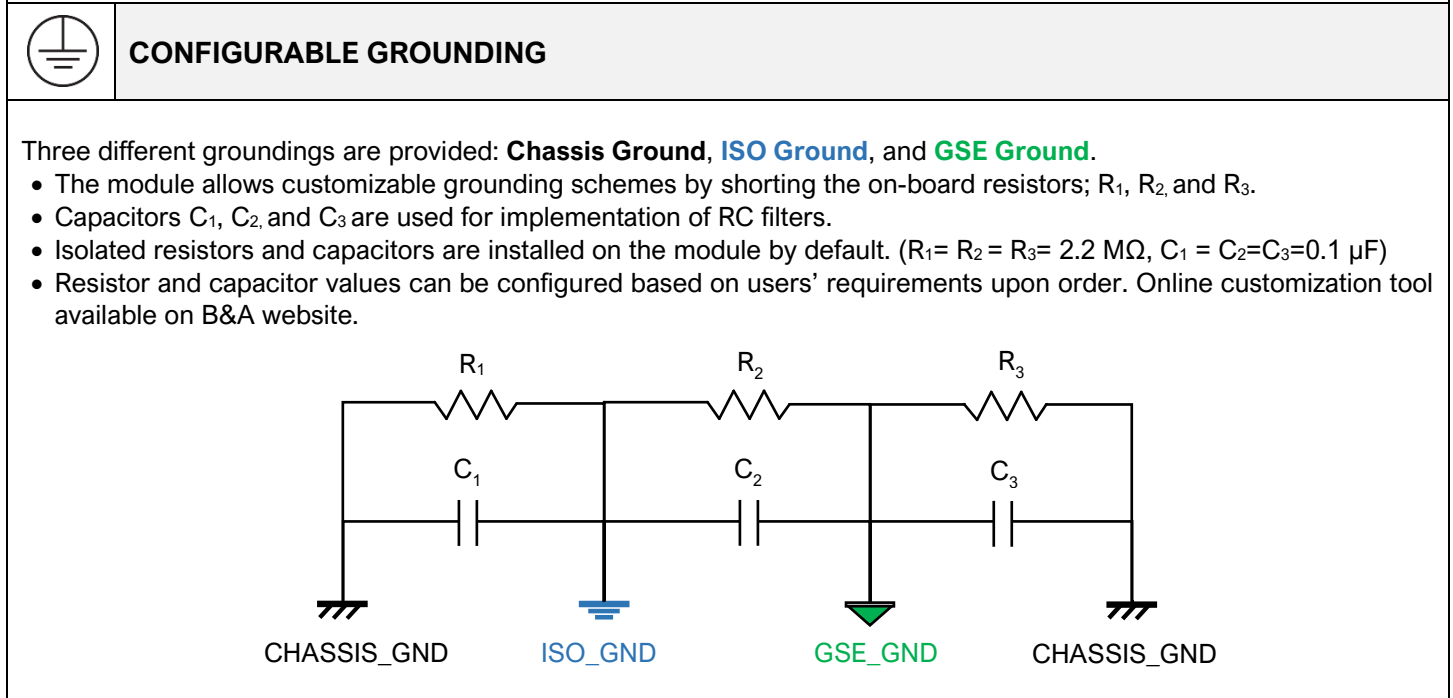
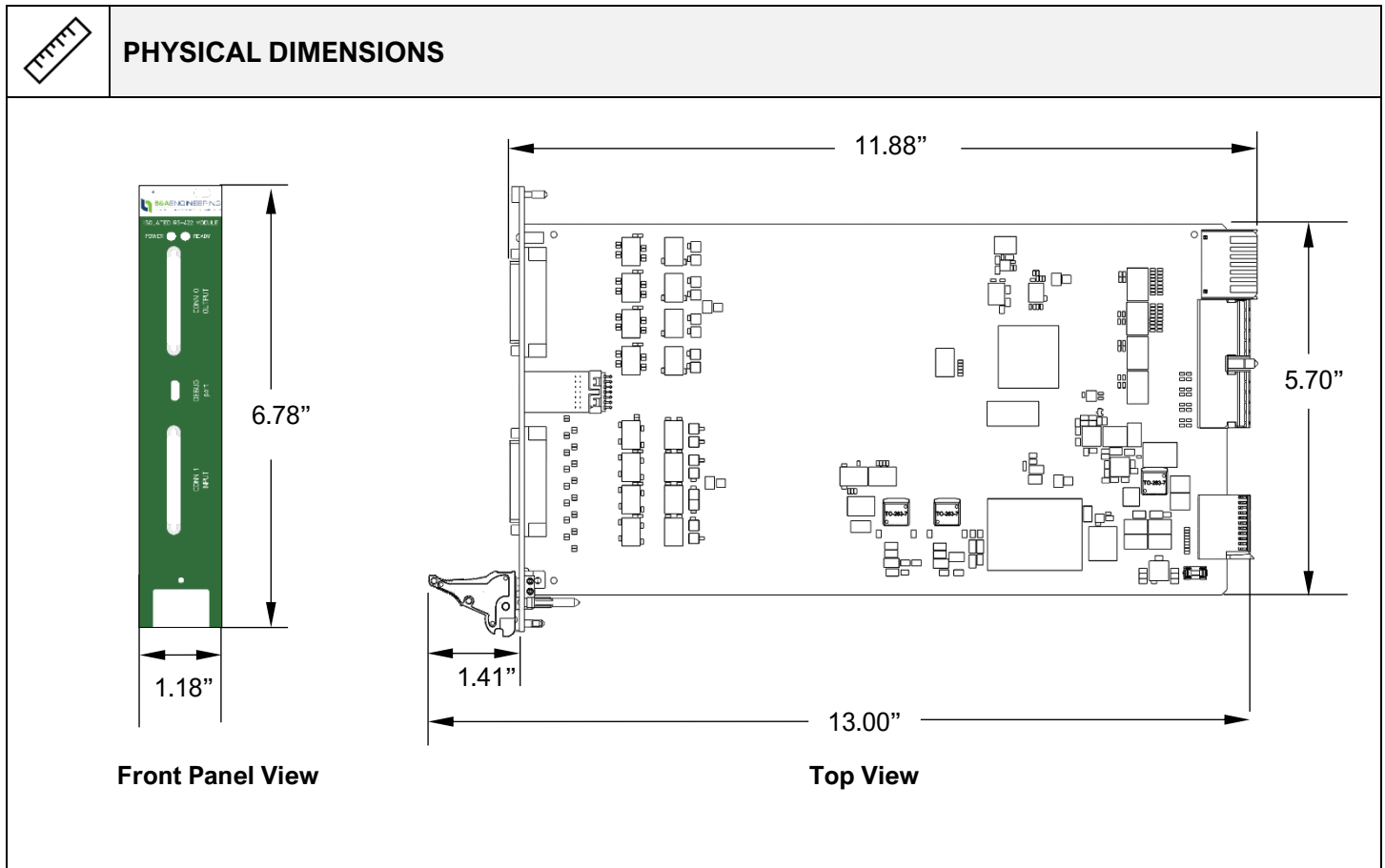
The functional block diagram is shown below:



ISOLATED VOLTAGE REGULATION

The Isolated Voltage Regulation block diagram is shown below:







PROPAGATION DELAY

The propagation delay is defined as the delay between the 50% trigger point and the 50% response point. The figure below defines two different propagation delays: The LOW to HIGH signal rise phase (LH) and HIGH to LOW signal Drop phase (HL). The signal rise and drop measurement is performed bi-directional for the TX and RX propagation direction. An Oscilloscope is required to perform testing. The signal data is measured with the oscilloscope at the board INPUT, TX output, RX input, and board OUTPUT. For delay measurements, ISO_GND and GSE_GND are connected.

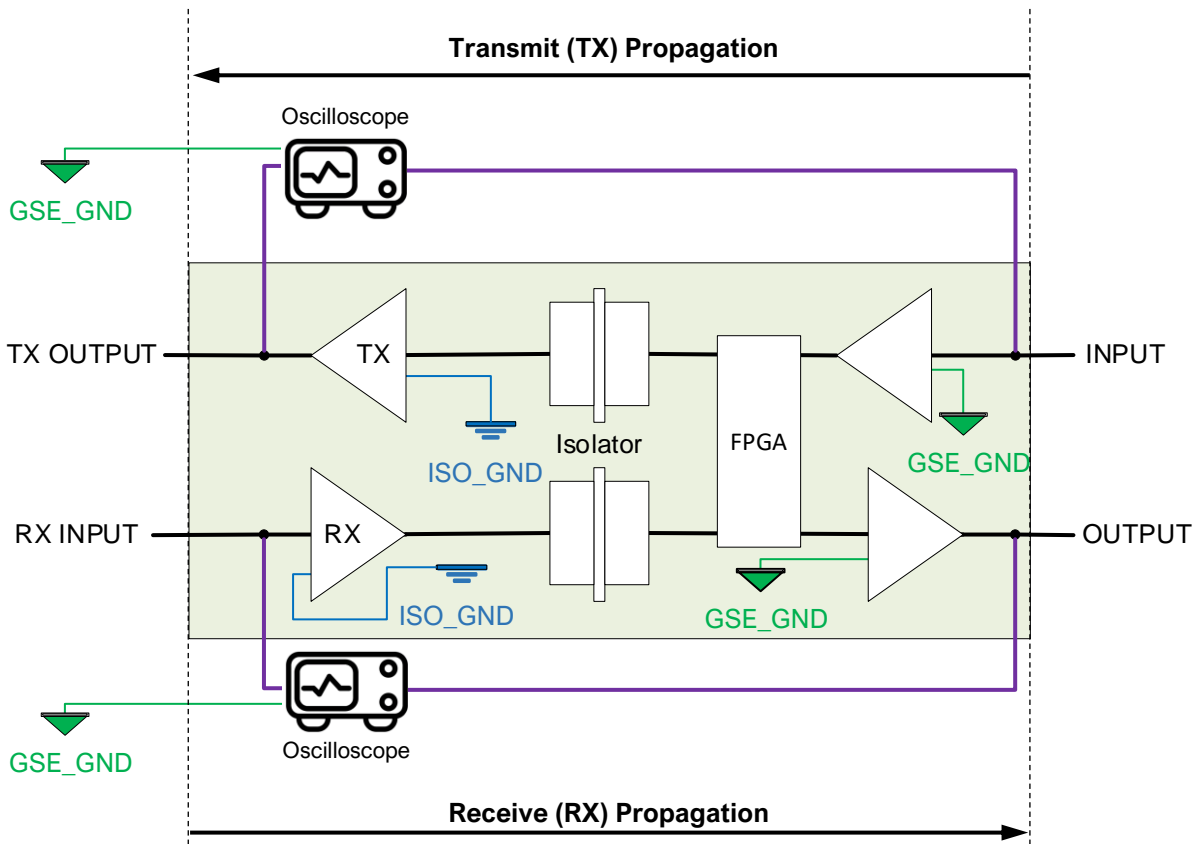
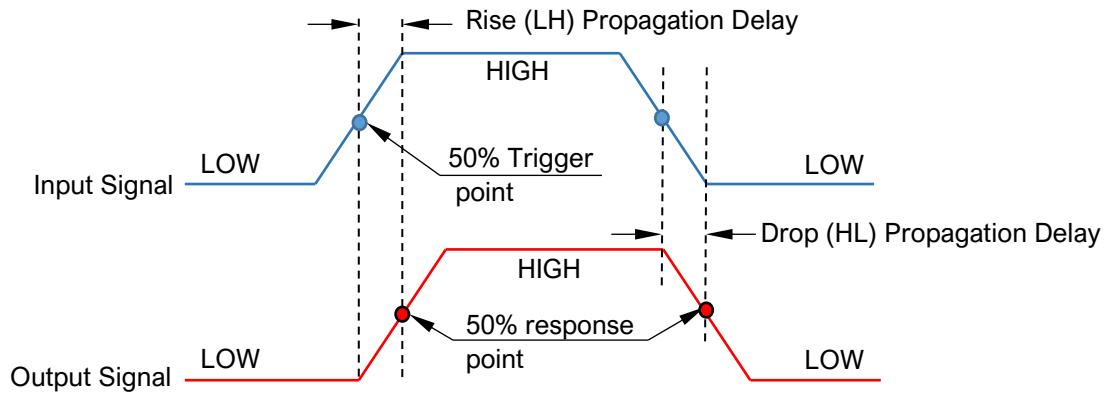
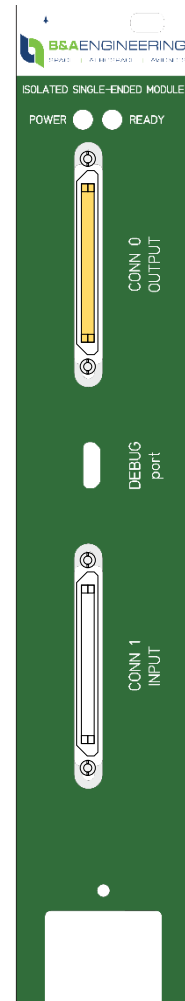


Table 1. ISOLATED SINGLE ENDED MODULE (LVTTTL) CONN 0 PINOUT

ISO_GND	68	34	ISO_GND
TX_31	67	33	TX_15
ISO_GND	66	32	ISO_GND
TX_30	65	31	TX_14
ISO_GND	64	30	ISO_GND
TX_29	63	29	TX_13
ISO_GND	62	28	ISO_GND
TX_28	61	27	TX_12
ISO_GND	60	26	ISO_GND
ISO_GND	59	25	ISO_GND
TX_27	58	24	TX_11
ISO_GND	57	23	ISO_GND
TX_26	56	22	TX_10
ISO_GND	55	21	ISO_GND
TX_25	54	20	TX_9
ISO_GND	53	19	ISO_GND
TX_24	52	18	TX_8
ISO_GND	51	17	ISO_GND
TX_23	50	16	TX_7
ISO_GND	49	15	ISO_GND
TX_22	48	14	TX_6
ISO_GND	47	13	ISO_GND
TX_21	46	12	TX_5
ISO_GND	45	11	ISO_GND
TX_20	44	10	TX_4
ISO_GND	43	9	ISO_GND
ISO_GND	42	8	ISO_GND
TX_19	41	7	TX_3
ISO_GND	40	6	ISO_GND
TX_18	39	5	TX_2
ISO_GND	38	4	ISO_GND
TX_17	37	3	TX_1
ISO_GND	36	2	ISO_GND
TX_16	35	1	TX_0



DATA SHEET

Table 2. ISOLATED SINGLE ENDED MODULE (LVTTTL) CONN 1 PINOUT

ISO_GND	68	34	ISO_GND
RX_31	67	33	RX_15
ISO_GND	66	32	ISO_GND
RX_30	65	31	RX_14
ISO_GND	64	30	ISO_GND
RX_29	63	29	RX_13
ISO_GND	62	28	ISO_GND
RX_28	61	27	RX_12
ISO_GND	60	26	ISO_GND
ISO_GND	59	25	ISO_GND
RX_27	58	24	RX_11
ISO_GND	57	23	ISO_GND
RX_26	56	22	RX_10
ISO_GND	55	21	ISO_GND
RX_25	54	20	RX_9
ISO_GND	53	19	ISO_GND
RX_24	52	18	RX_8
ISO_GND	51	17	ISO_GND
RX_23	50	16	RX_7
ISO_GND	49	15	ISO_GND
RX_22	48	14	RX_6
ISO_GND	47	13	ISO_GND
RX_21	46	12	RX_5
ISO_GND	45	11	ISO_GND
RX_20	44	10	RX_4
ISO_GND	43	9	ISO_GND
ISO_GND	42	8	ISO_GND
RX_19	41	7	RX_3
ISO_GND	40	6	ISO_GND
RX_18	39	5	RX_2
ISO_GND	38	4	ISO_GND
RX_17	37	3	RX_1
ISO_GND	36	2	ISO_GND
RX_16	35	1	RX_0

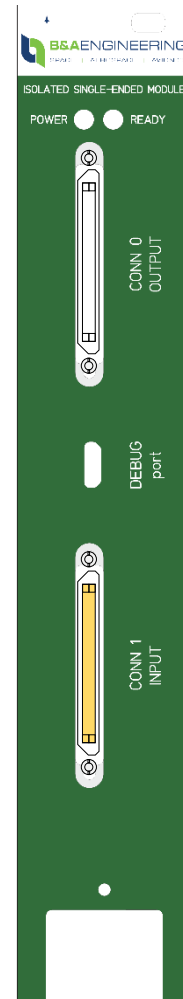
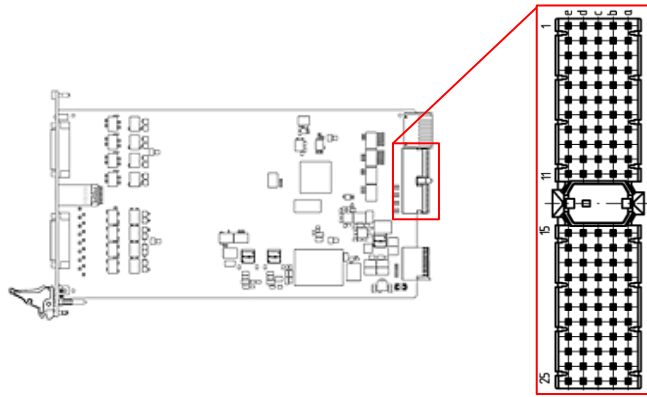
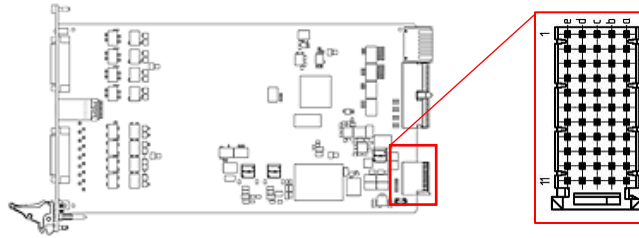


Table 3. Backplane 110P XJ2 Connector Pinout



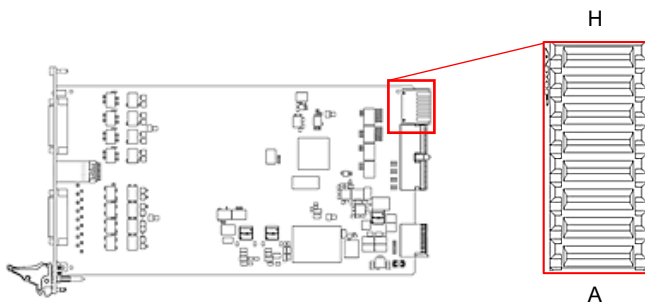
	e	d	c	b	a
1	OUT_3	OUT_2	CLK_OUT_0_IN	OUT_1	OUT_0
2	OUT_7	OUT_6	N/C	OUT_5	OUT_4
3	GSE_GND	GSE_GND	GSE_GND	GSE_GND	GSE_GND
4	OUT_11	OUT_10	N/C	OUT_9	OUT_8
5	OUT_15	OUT_14	N/C	OUT_13	OUT_12
6	GSE_GND	GSE_GND	GSE_GND	GSE_GND	GSE_GND
7	OUT_19	OUT_18	N/C	OUT_17	OUT_16
8	OUT_23	OUT_22	N/C	OUT_21	OUT_20
9	GSE_GND	GSE_GND	GSE_GND	GSE_GND	GSE_GND
10	OUT_27	OUT_26	N/C	OUT_25	OUT_24
11	OUT_31	OUT_30	N/C	OUT_29	OUT_28
12	GSE_GND	GSE_GND	GSE_GND	GSE_GND	GSE_GND
13	N/C	N/C	N/C	N/C	N/C
14	N/C	N/C	N/C	N/C	N/C
15	IN_3	IN_2	CLK_IN_0_IN	IN_1	IN_0
16	IN_7	IN_6	N/C	IN_5	IN_4
17	GSE_GND	GSE_GND	GSE_GND	GSE_GND	GSE_GND
18	IN_11	IN_10	N/C	IN_9	IN_8
19	IN_15	IN_14	N/C	IN_13	IN_12
20	GSE_GND	GSE_GND	GSE_GND	GSE_GND	GSE_GND
21	IN_19	IN_18	N/C	IN_17	IN_16
22	IN_23	IN_22	N/C	IN_21	IN_20
23	GSE_GND	GSE_GND	GSE_GND	GSE_GND	GSE_GND
24	IN_27	IN_26	N/C	IN_25	IN_24
25	IN_31	IN_30	N/C	IN_29	IN_28

Table 4. Backplane 55P XJ1 Connector Pinout



	f	e	d	c	b	a
1	GSE_GND	N/C	N/C	N/C	N/C	N/C
2	GSE_GND	N/C	N/C	N/C	N/C	N/C
3	GSE_GND	N/C	N/C	N/C	N/C	N/C
4	GSE_GND	N/C	N/C	N/C	N/C	N/C
5	GSE_GND	N/C	N/C	N/C	N/C	N/C
6	GSE_GND	N/C	N/C	N/C	N/C	N/C
7	GSE_GND	GSE_GND	N/C	GSE_GND	N/C	GSE_GND
8	GSE_GND	SLSC_SpiMosi	GSE_GND	SLSC_SpiCLK	GSE_GND	SLSC_InitIn#
9	GSE_GND	GSE_GND	SLSC_Trig_To_Mod	GSE_GND	SLSC_Tri_From_Mod	GSE_GND
10	GSE_GND	N/C	GSE_GND	SLSC_SpiMiso	GSE_GND	SLSC_ED_SS#
11	GSE_GND	24 V	SLSC Rdy/Rst#	3.3V	SLSC ID SS#	24 V

Table 5. Backplane XJ3 Connector Pinout



H	ISO_GND
G	ISO_GND
F	EXT_CLK_IN
E	EXT_CLK_OUT
D	CHASSIS_GND
C	CHASSIS_GND
B	GSE_GND
A	GSE_GND