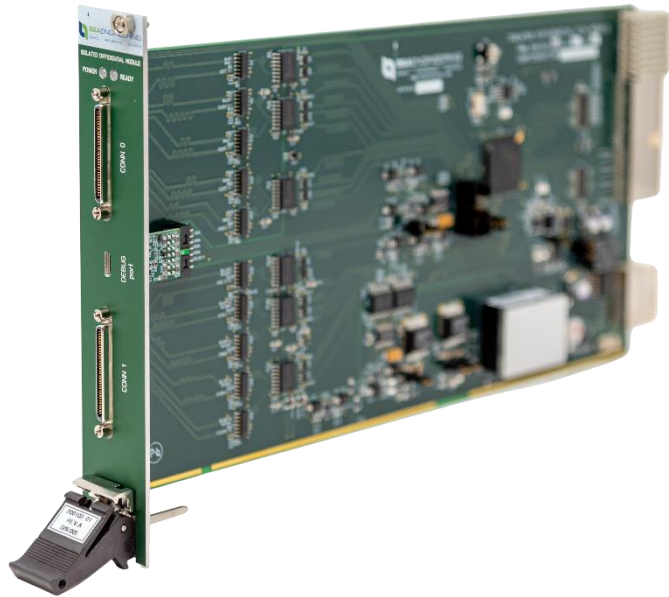


# LVDS / mLVDS/ RS-485 SLSC Module



**Product Data Sheet**  
B&A Document 110031\_A

Part No.200102-X\_A  
OCT 2022



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## INTRODUCTION

This document contains technical specifications for the LVDS/MLVDS/RS-485 Module (Part # 200102-X\_A). Specifications are shown at 25 °C temperature, unless otherwise noted. The main features are listed below:

- Separate 16 Transmit and 16 Receive configurable LVDS/MLVDS/RS-485 full duplex channels.
- (See page 9 of datasheet for available configurations)
- Configurable grounding
- On-board Isolated voltage regulation
- Internal House Keeping / Health Monitoring
- User controlled Flight interface power on/off
- Built-in LabVIEW FPGA Debugging Port
- Safe to connect to Flight hardware, FMEA approved
- LabVIEW drivers



## DIGITAL I/O

Front panel Connectors	2 x VHDCI (Tables 1 & 2)
Channels Per Connector <sup>1</sup>	18
Maximum Nominal Data Rate of TX and RX Channels	200 Mbps
Number of TX Channels	16+2
Number of RX Channels	16+2
Backplane Connectors	3 x SLSC (Tables 3-5)
TX LH Propagation Delay (ns) <sup>2</sup> Min, Avg, Max	24, 25, 26
TX HL Propagation Delay (ns) <sup>2</sup> Min, Avg, Max	24, 25, 26
RX LH Propagation Delay (ns) <sup>2</sup> Min, Avg, Max	25, 26, 27
RX HL Propagation Delay (ns) <sup>2</sup> Min, Avg, Max	25, 26, 27

### Note:

- (1) All 16 channels (TX and RX) are trace matched and have same delay on the board.
- (2) See Page 4 for propagation delay definitions.



## SAFETY

The following items must be considered for safety:

- Using the module in a manner not described within this document may impair the protection the module provides.
- The SLSC-12001 chassis and the SLSC cards **do not support** hot plug-in. The entire chassis must be powered down when a module is installed.
- Always follow ESD procedures for handling.
- If cleaning is required, wipe with dry and clean towel.
- Installation of the SLSC module must be performed in accordance with B&A “DIGITAL ISOLATION MODULE USER MANUAL.pdf” (Document No. 140020).



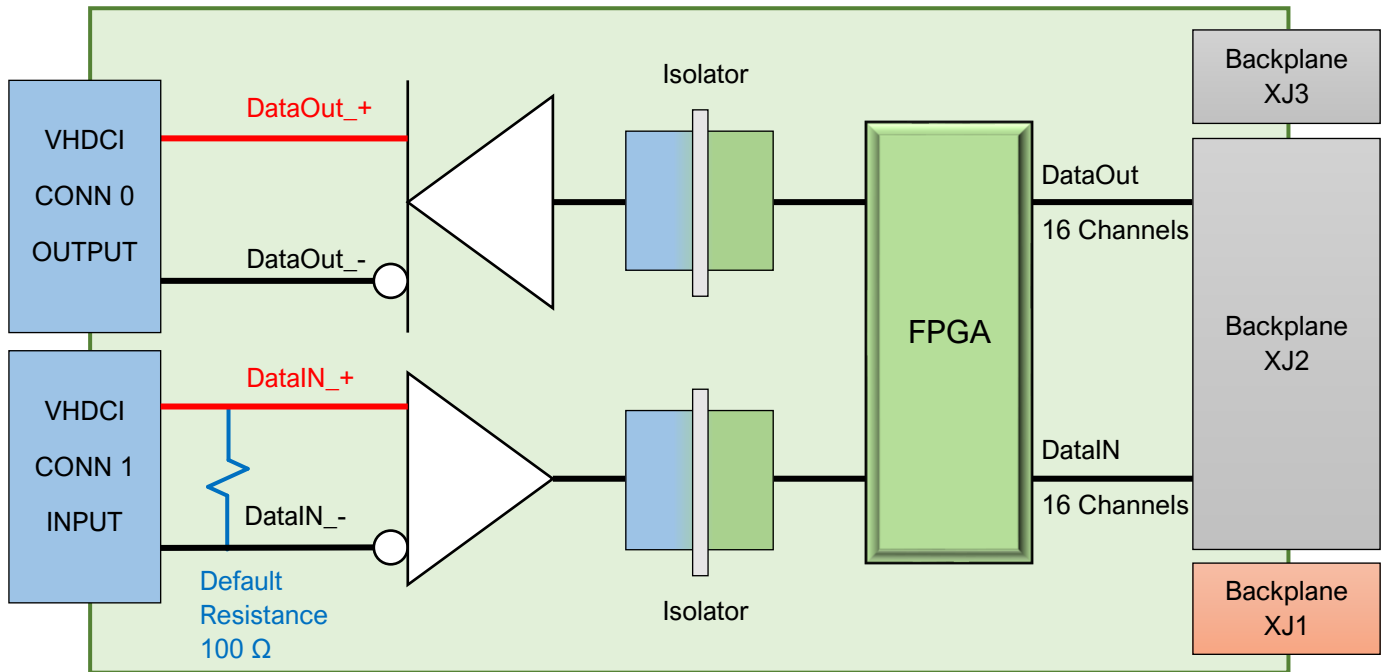
## SPECIFICATIONS

Direction Control of Data Channels	Full Duplex
Power Up State	Drivers and receivers disabled
I/O Compatibility	LVDS/ mLVDS/ RS 485 (differential)
Characteristic Impedance	100 Ω differential nominal 50 Ω single ended nominal
Termination Impedance	100 Ω differential nominal
Input Differential Voltage	0.05 V - 0.6 V
Maximum Common Mode Input Voltage	2.5 V
Number of on card Temperature Sensors	4
LabVIEW FPGA Debug Interface	Micro-USB
Grounding Configuration	See Page 3



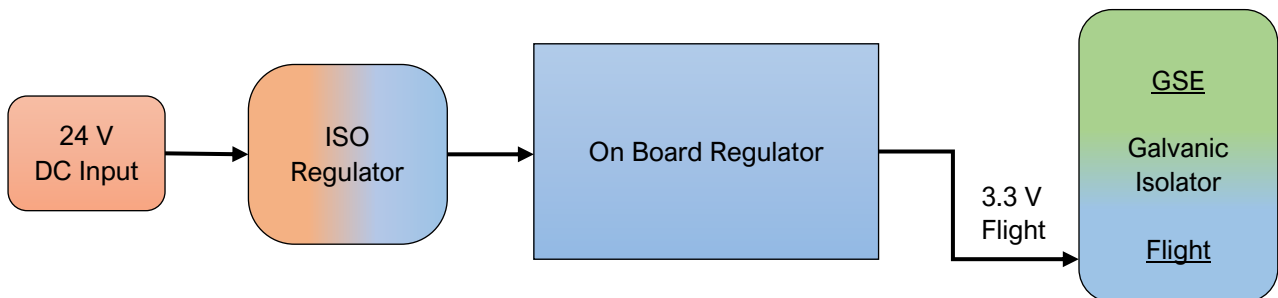
**FUNCTIONAL BLOCK DIAGRAM**

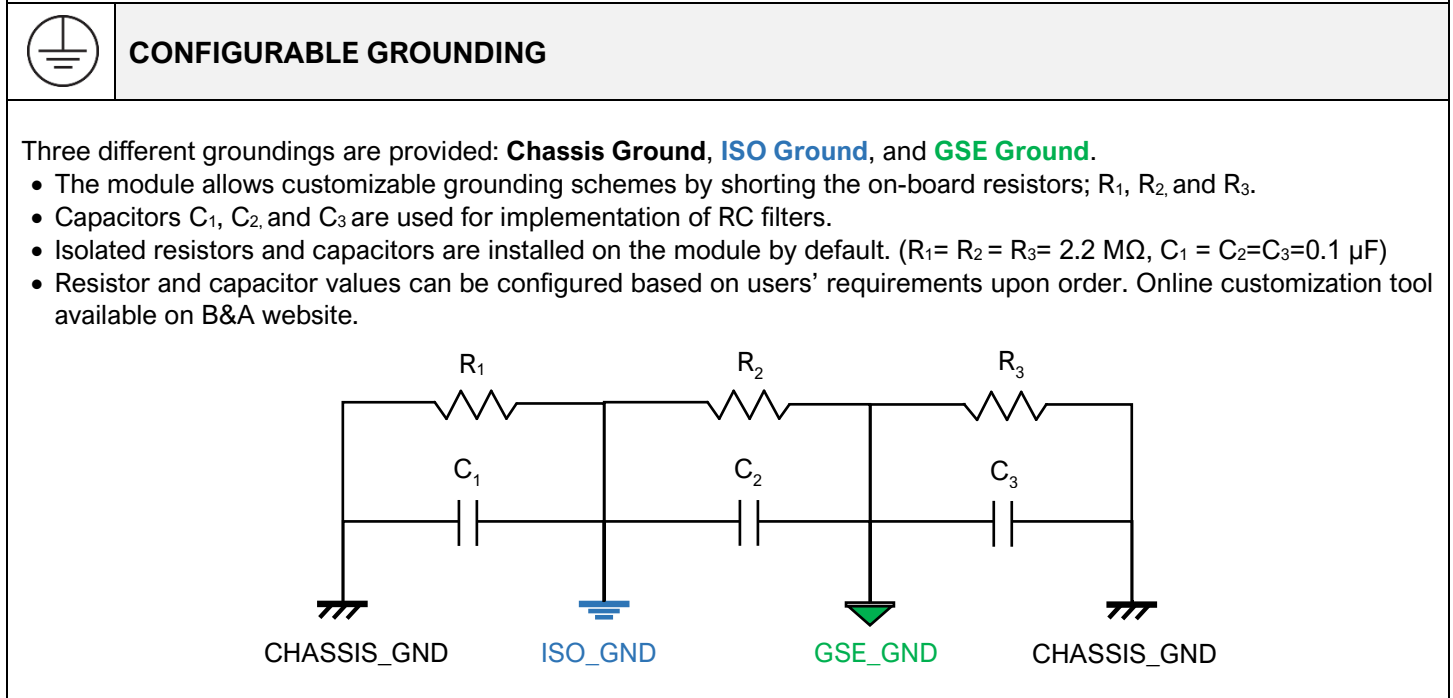
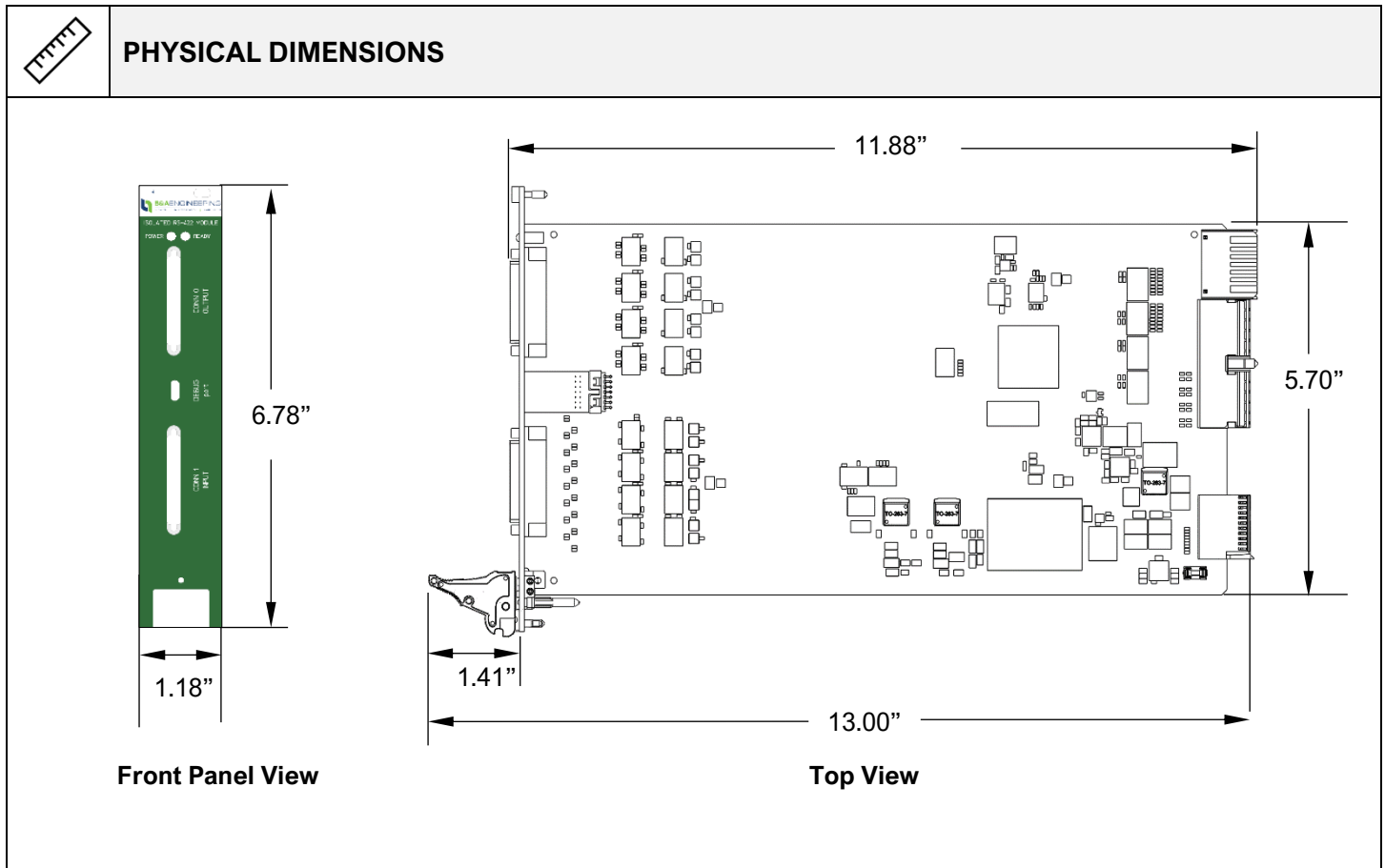
The functional block diagram is shown below:



**ISOLATED VOLTAGE REGULATION**

The Isolated Voltage Regulation block diagram is shown below:







**PROPAGATION DELAY**

The propagation delay is defined as the delay between the 50% trigger point and the 50% response point. The figure below defines two different propagation delays: The LOW to HIGH signal rise phase (LH) and HIGH to LOW signal Drop phase (HL). The signal rise and drop measurement is performed bi-directional for the TX and RX propagation direction. An Oscilloscope and Differential Probe (DP) are required to perform testing. The signal data is measured with the oscilloscope at the board INPUT, TX output, RX input, and board OUTPUT.

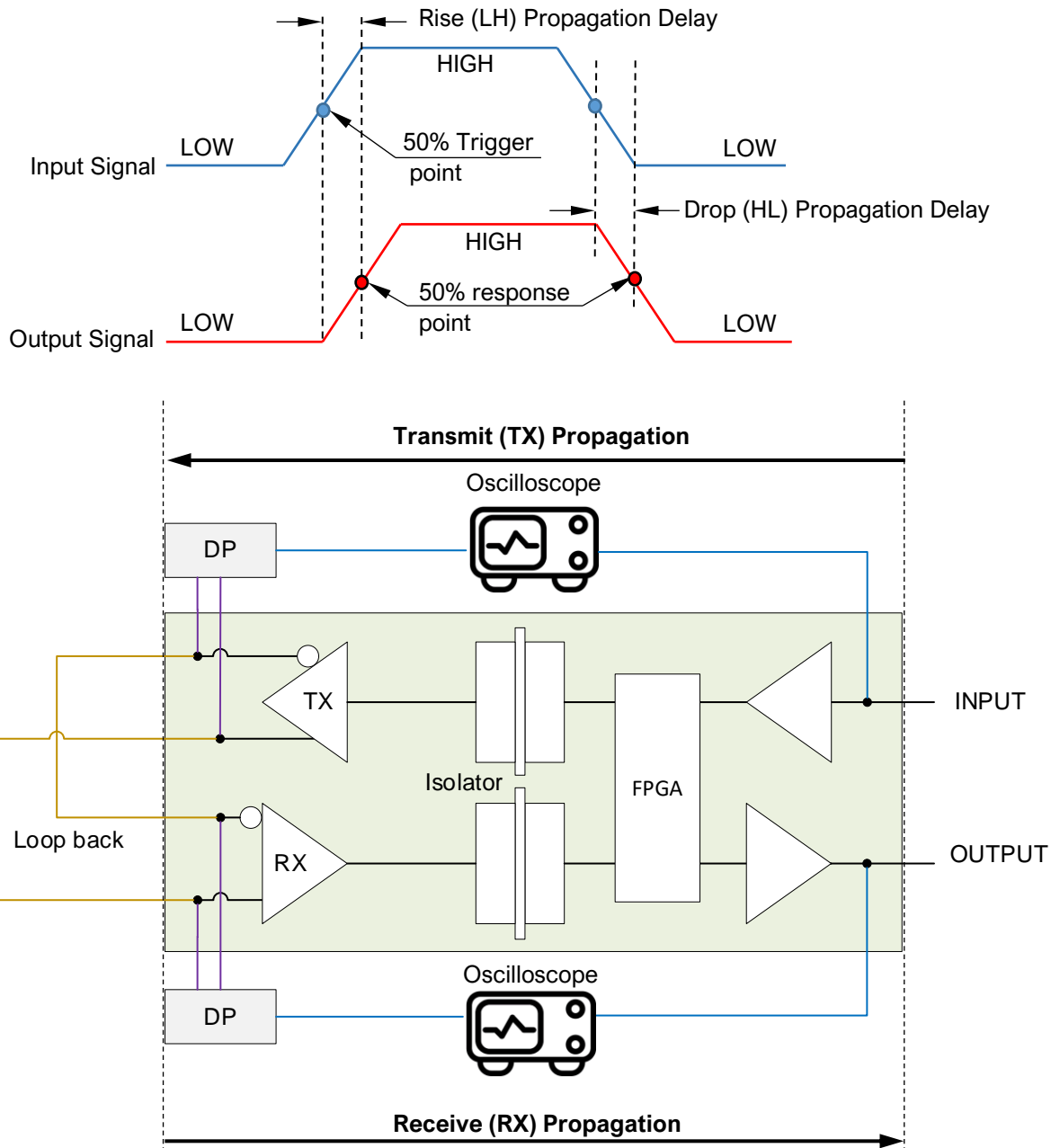


Table 1. Isolated Module CONN 0 Pinout (configured example shown for 16+2 LVDS and 16+2 mLVDS channels)

CLK_OUT_0+	68	34	CLK_OUT_0-
CLK_IN_0+	67	33	CLK_IN_0-
GND	66	32	GND
LVDS_TX_7+	65	31	LVDS_TX_7-
GND	64	30	GND
LVDS_RX_7+	63	29	LVDS_RX_7-
GND	62	28	GND
LVDS_TX_6+	61	27	LVDS_TX_6-
GND	60	26	GND
LVDS_RX_6+	59	25	LVDS_RX_6-
GND	58	24	GND
LVDS_TX_5+	57	23	LVDS_TX_5-
GND	56	22	GND
LVDS_RX_5+	55	21	LVDS_RX_5-
GND	54	20	GND
LVDS_TX_4+	53	19	LVDS_TX_4-
GND	52	18	GND
LVDS_RX_4+	51	17	LVDS_RX_4-
GND	50	16	GND
LVDS_TX_3+	49	15	LVDS_TX_3-
GND	48	14	GND
LVDS_RX_3+	47	13	LVDS_RX_3-
GND	46	12	GND
LVDS_TX_2+	45	11	LVDS_TX_2-
GND	44	10	GND
LVDS_RX_2+	43	9	LVDS_RX_2-
GND	42	8	GND
LVDS_TX_1+	41	7	LVDS_TX_1-
GND	40	6	GND
LVDS_RX_1+	39	5	LVDS_RX_1-
GND	38	4	GND
LVDS_TX_0+	37	3	LVDS_TX_0-
GND	36	2	GND
LVDS_RX_0+	35	1	LVDS_RX_0-

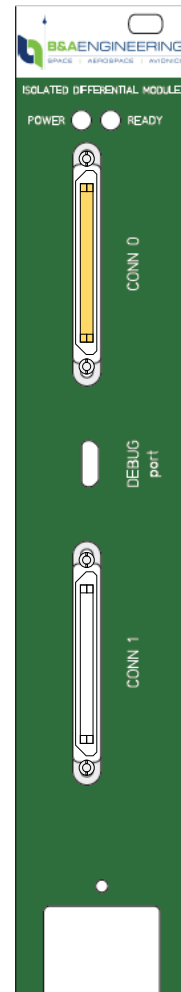


Table 2. Isolated Module CONN 1 Pinout (configured example shown for 16+2 LVDS and 16+2 mLVDS channels)

CLK_IN_1+	68	34	CLK_IN_1+
CLK_OUT_1+	67	33	CLK_OUT_1+
GND	66	32	GND
MLVDS_RX_7+	65	31	MLVDS_RX_7-
GND	64	30	GND
MLVDS_TX_7+	63	29	MLVDS_TX_7-
GND	62	28	GND
MLVDS_RX_6+	61	27	MLVDS_RX_6-
GND	60	26	GND
MLVDS_TX_6+	59	25	MLVDS_TX_6-
GND	58	24	GND
MLVDS_RX_5+	57	23	MLVDS_RX_5-
GND	56	22	GND
MLVDS_TX_5+	55	21	MLVDS_TX_5-
GND	54	20	GND
MLVDS_RX_4+	53	19	MLVDS_RX_4-
GND	52	18	GND
MLVDS_TX_4+	51	17	MLVDS_TX_4-
GND	50	16	GND
MLVDS_RX_3+	49	15	MLVDS_RX_3-
GND	48	14	GND
MLVDS_TX_3+	47	13	MLVDS_TX_3-
GND	46	12	GND
MLVDS_RX_2+	45	11	MLVDS_RX_2-
GND	44	10	GND
MLVDS_TX_2+	43	9	MLVDS_TX_2-
GND	42	8	GND
MLVDS_RX_1+	41	7	MLVDS_RX_1-
GND	40	6	GND
MLVDS_TX_1+	39	5	MLVDS_TX_1-
GND	38	4	GND
MLVDS_RX_0+	37	3	MLVDS_RX_0-
GND	36	2	GND
MLVDS_TX_0+	35	1	MLVDS_TX_0-

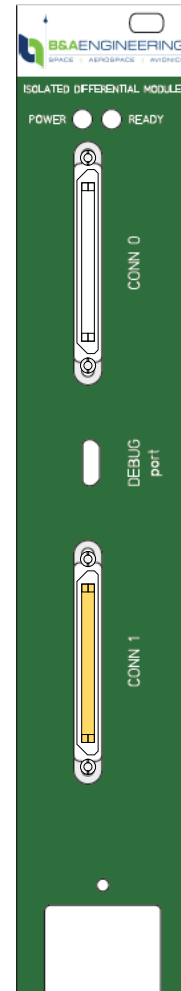
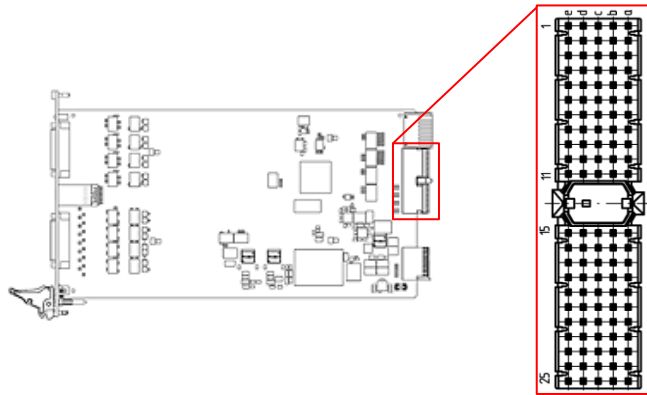




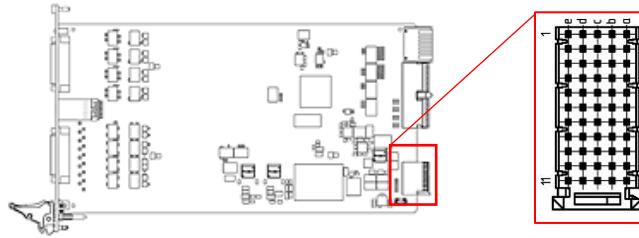
Table 3. Backplane 110P XJ2 Connector Pinout



	e	d	c	b	a
1	OUT_3	OUT_2	CLK_OUT_0_IN	OUT_1	OUT_0
2	OUT_7	OUT_6	N/C	OUT_5	OUT_4
3	GND	GND	GND	GND	GND
4	OUT_11	OUT_10	N/C	OUT_9	OUT_8
5	OUT_15	OUT_14	N/C	OUT_13	OUT_12
6	GND	GND	GND	GND	GND
7	OUT_19	OUT_18	N/C	OUT_17	OUT_16
8	OUT_23	OUT_22	N/C	OUT_21	OUT_20
9	GND	GND	GND	GND	GND
10	OUT_27	OUT_26	N/C	OUT_25	OUT_24
11	OUT_31	OUT_30	N/C	OUT_29	OUT_28
12	GND	GND	GND	GND	GND
13	N/C	N/C	N/C	N/C	N/C
14	N/C	N/C	N/C	N/C	N/C
15	IN_3	IN_2	CLK_IN_0_IN	IN_1	IN_0
16	IN_7	IN_6	N/C	IN_5	IN_4
17	GND	GND	GND	GND	GND
18	IN_11	IN_10	N/C	IN_9	IN_8
19	IN_15	IN_14	N/C	IN_13	IN_12
20	GND	GND	GND	GND	GND
21	IN_19	IN_18	N/C	IN_17	IN_16
22	IN_23	IN_22	N/C	IN_21	IN_20
23	GND	GND	GND	GND	GND
24	IN_27	IN_26	N/C	IN_25	IN_24
25	IN_31	IN_30	N/C	IN_29	IN_28

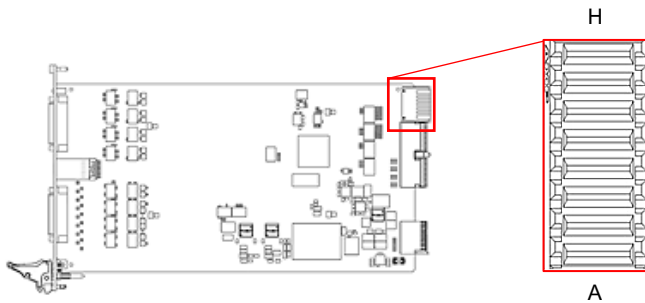


**Table 4. Backplane 55P XJ1 Connector Pinout**



	f	e	d	c	b	a
1	GSE_GND	N/C	N/C	N/C	N/C	N/C
2	GSE_GND	N/C	N/C	N/C	N/C	N/C
3	GSE_GND	N/C	N/C	N/C	N/C	N/C
4	GSE_GND	N/C	N/C	N/C	N/C	N/C
5	GSE_GND	N/C	N/C	N/C	N/C	N/C
6	GSE_GND	N/C	N/C	N/C	N/C	N/C
7	GSE_GND	GSE_GND	N/C	GSE_GND	N/C	GSE_GND
8	GSE_GND	SLSC_SpiMosi	GSE_GND	SLSC_SpiCLK	GSE_GND	SLSC_InitIn#
9	GSE_GND	GSE_GND	SLSC_Trig_To_Mod	GSE_GND	SLSC_Tri_From_Mod	GSE_GND
10	GSE_GND	N/C	GSE_GND	SLSC_SpiMiso	GSE_GND	SLSC_ED_SS#
11	GSE_GND	24 V	SLSC Rdy/Rst#	3.3V	SLSC ID SS#	24 V

**Table 5. Backplane XJ3 Connector Pinout**



H	ISO_GND
G	ISO_GND
F	EXT_CLK_IN
E	EXT_CLK_OUT
D	CHASSIS_GND
C	CHASSIS_GND
B	GSE_GND
A	GSE_GND

## ORDERING INFORMATION

When ordering please specify the requested part number shown in Table 6.

For custom orders (200102-X), please provide the required LVDS / mLVDS / RS-485 channels. A dash number will be associated with the requested configuration.

**Table 6.** Dash number for available configurations

Part No.	Product Description
200102-00	ISOLATED DIFFERENTIAL SLSC MODULE (RS-485)
200102-01	ISOLATED DIFFERENTIAL SLSC MODULE (LVDS)
200102-02	ISOLATED DIFFERENTIAL SLSC MODULE (mLVDS)
200102-X	ISOLATED DIFFERENTIAL SLSC MODULE (Custom LVDS/mLVDS)